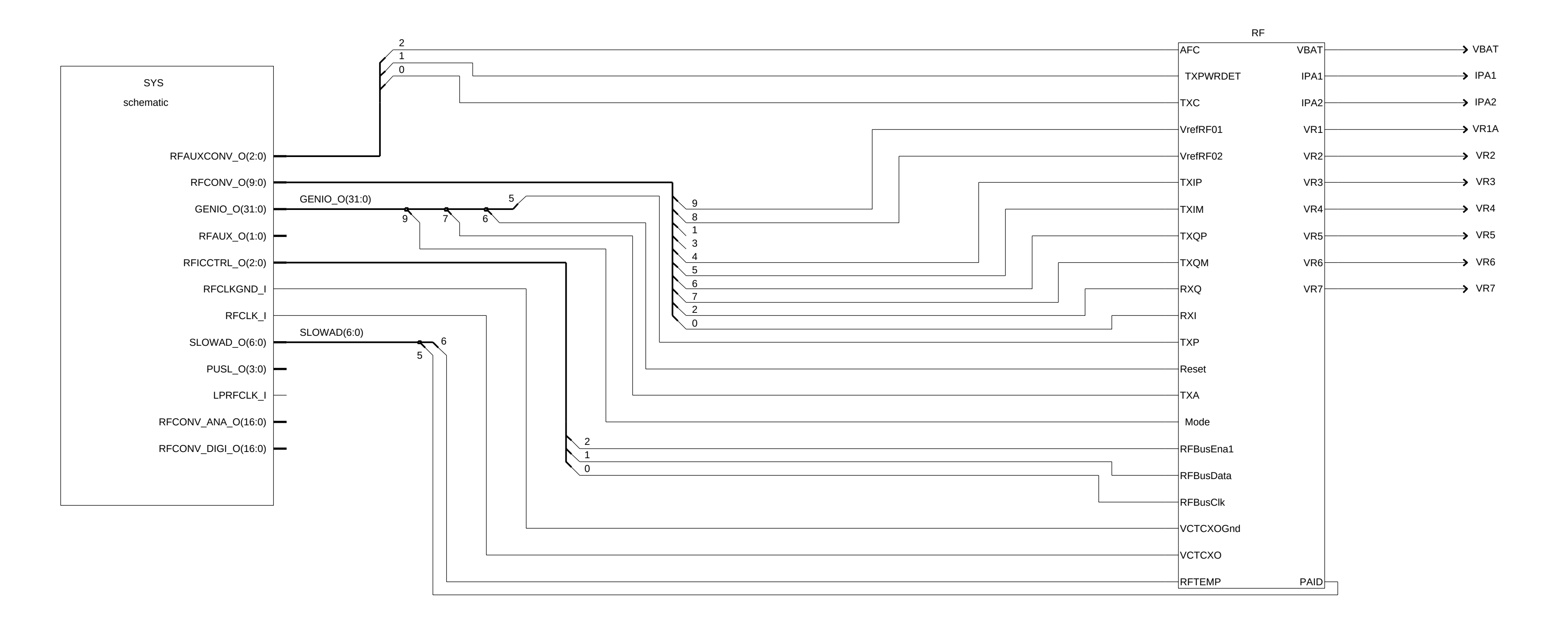
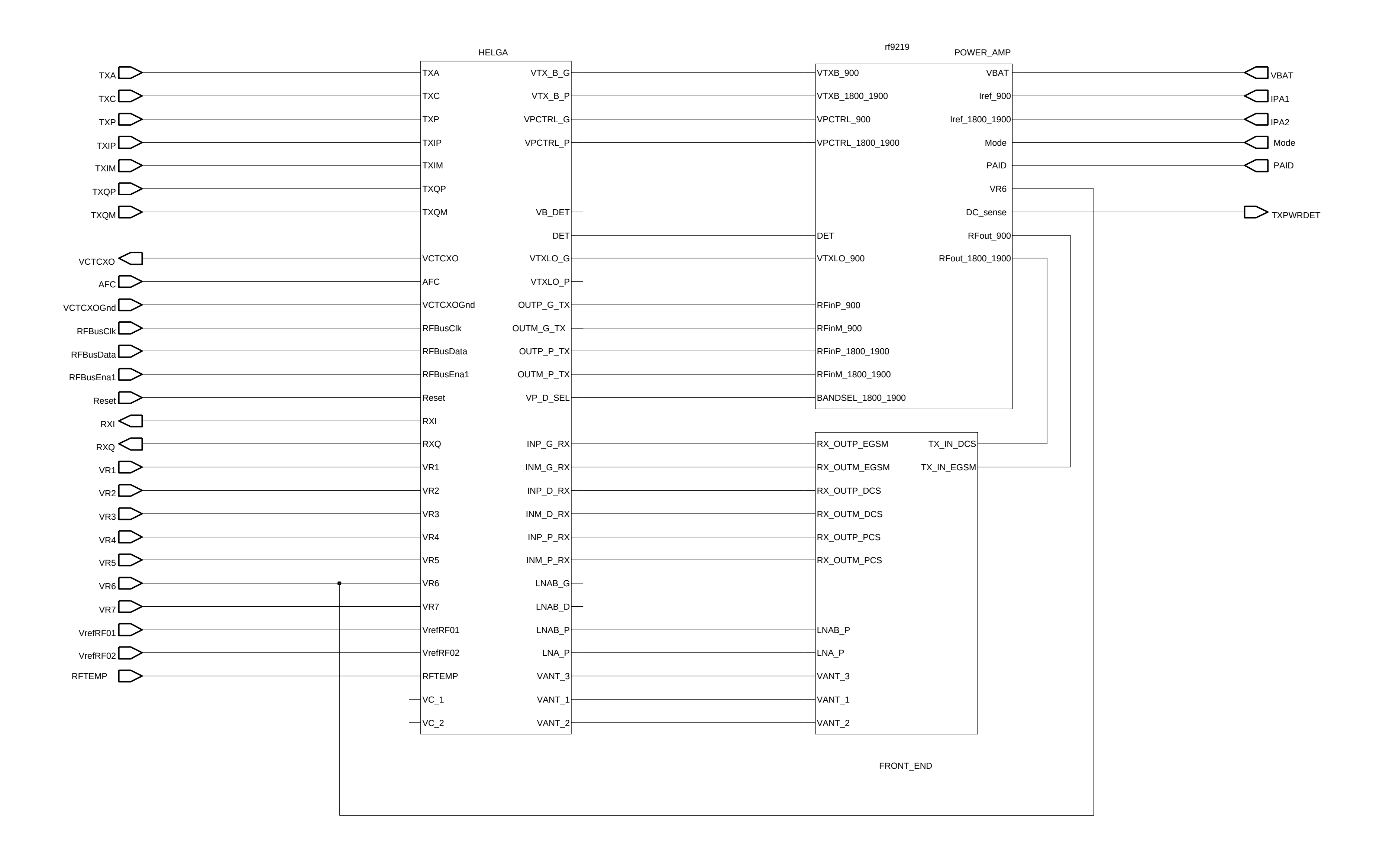
Top level

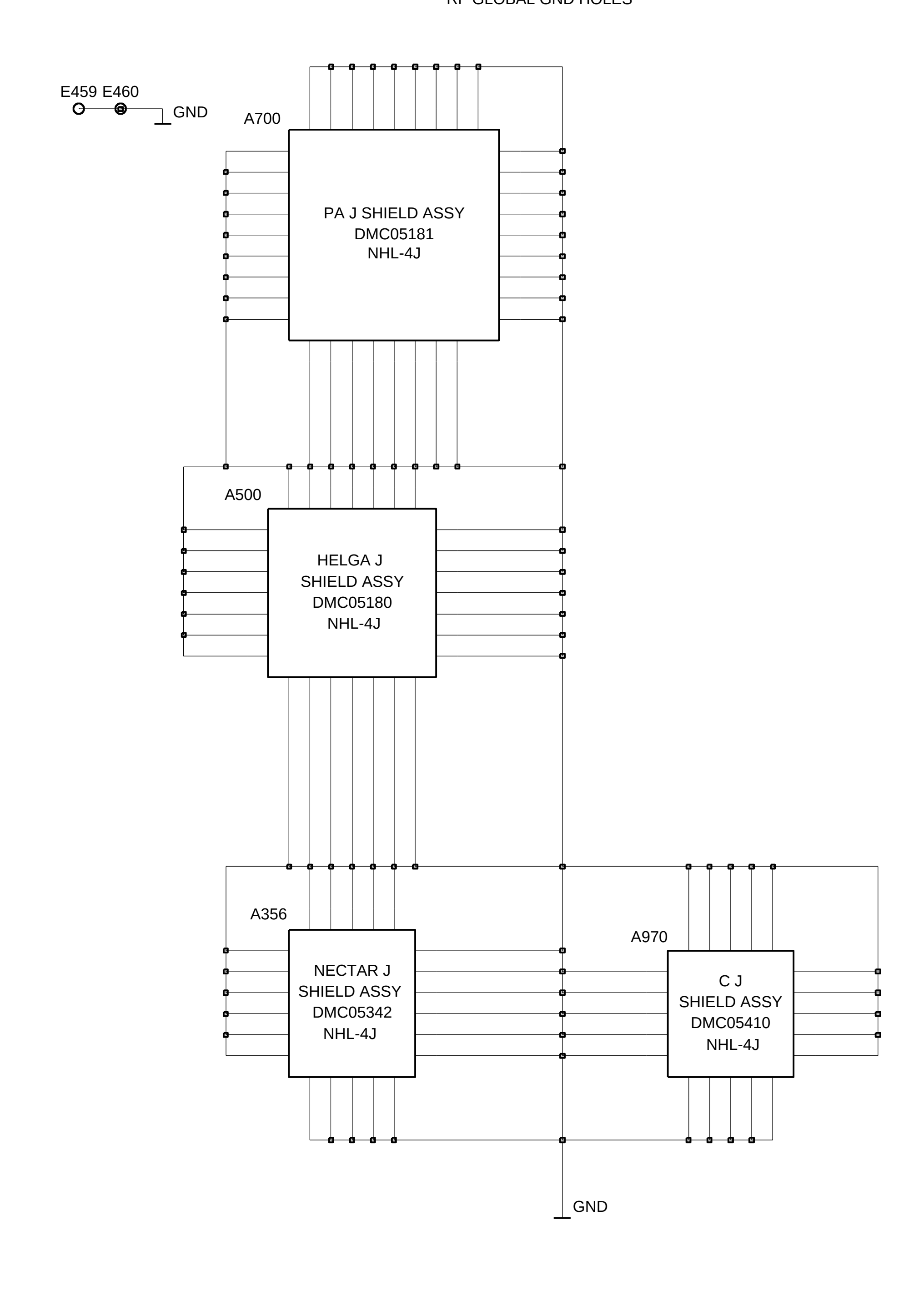

SYS
schematic
RFAUXCONV_O(2:0)
RFCONV_O(9:0)
GENIO_O(31:0)
RFAUX_O(1:0)
RFICCTRL_O(2:0)
RFCLKGND_I
RFCLK_I
SLOWAD_O(6:0)
PUSL_O(3:0)
LPRFCLK_I
RFCONV_ANA_O(16:0)
RFCONV_DIGI_O(16:0)
GENIO_O(31:0)
SLOWAD(6:0)
RF
AFC
TXPWRDET
TXC
VrefRF01
VrefRF02
TXIP
TXIM
TXQP
TXQM
RXQ
RXI
TXP
Reset
TXA
Mode
RFBusEna1
RFBusData
RFBusClk
VCTCXOGnd
VCTCXO
RFTEMP
VBAT
IPA1
IPA2
VR1
VR2
VR3
VR4
VR5
VR6
VR7
PAID
VBAT
IPA1
IPA2
VR1A
VR2
VR3
VR4
VR5
VR6
VR7

RF Top level

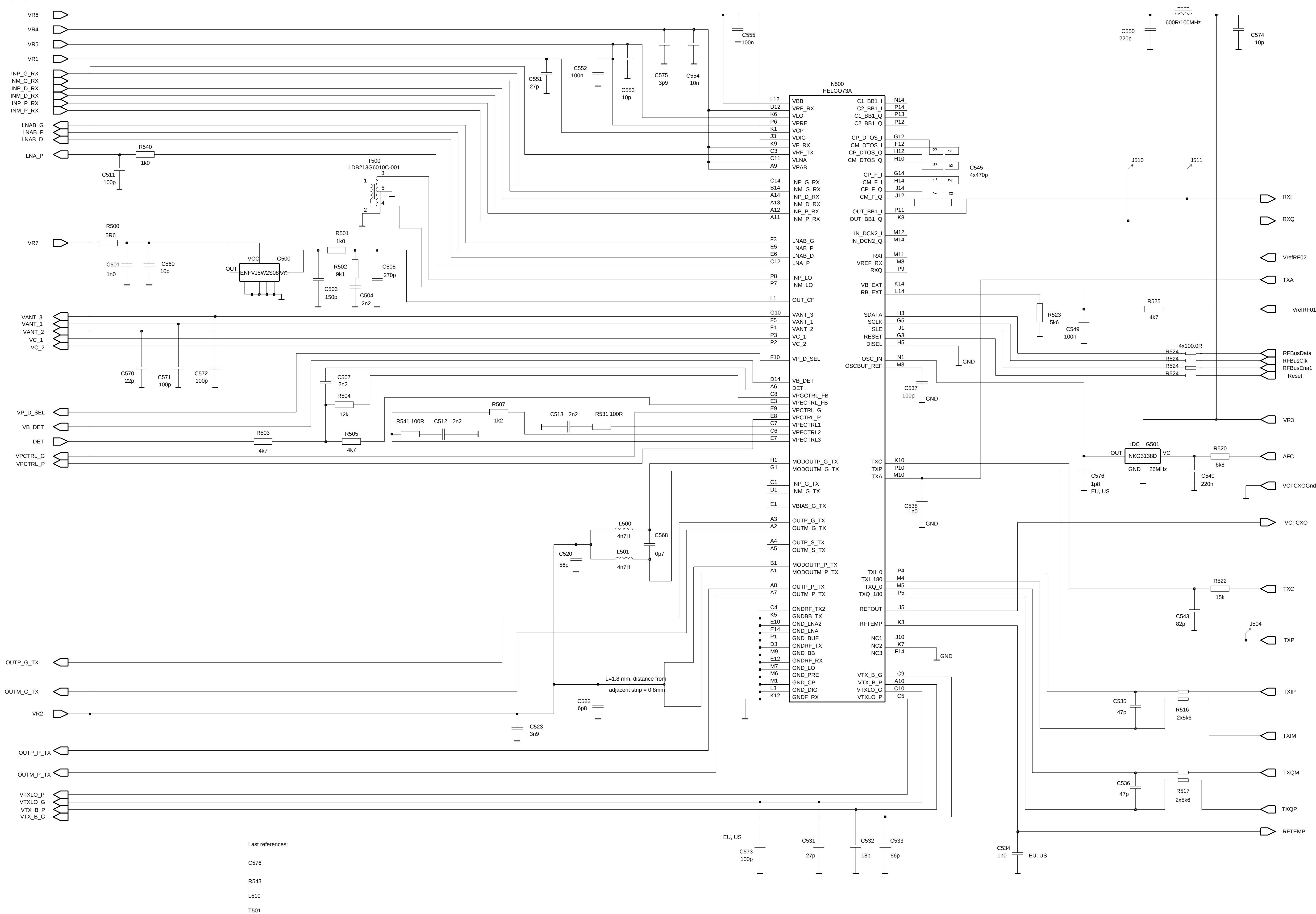


HELGA
rf9219
POWER_AMP
FRONT_END
TXA
TXC
TXP
TXIP
TXIM
TXQP
TXQM
VCTCXO
AFC
VCTCXOGnd
RFBusClk
RFBusData
RFBusEna1
Reset
RXI
RXQ
VR1
VR2
VR3
VR4
VR5
VR6
VR7
VrefRF01
VrefRF02
RFTEMP
VC_1
VC_2
VTX_B_G
VTX_B_P
VPCTRL_G
VPCTRL_P
VB_DET
DET
VTXLO_G
VTXLO_P
OUTP_G_TX
OUTM_G_TX
OUTP_P_TX
OUTM_P_TX
VP_D_SEL
INP_G_RX
INM_G_RX
INP_D_RX
INM_D_RX
INP_P_RX
INM_P_RX
LNAB_G
LNAB_D
LNAB_P
LNA_P
VANT_3
VANT_1
VANT_2
VTXB_900
VTXB_1800_1900
VPCTRL_900
VPCTRL_1800_1900
VTXLO_900
RFinP_900
RFinM_900
RFinP_1800_1900
RFinM_1800_1900
BANDSEL_1800_1900
VBAT
Iref_900
Iref_1800_1900
Mode
PAID
DC_sense
RFout_900
RFout_1800_1900
RX_OUTP_EGSM
RX_OUTM_EGSM
RX_OUTP_DCS
RX_OUTM_DCS
RX_OUTP_PCS
RX_OUTM_PCS
TX_IN_DCS
TX_IN_EGSM
IPA1
IPA2
TXPWRDET

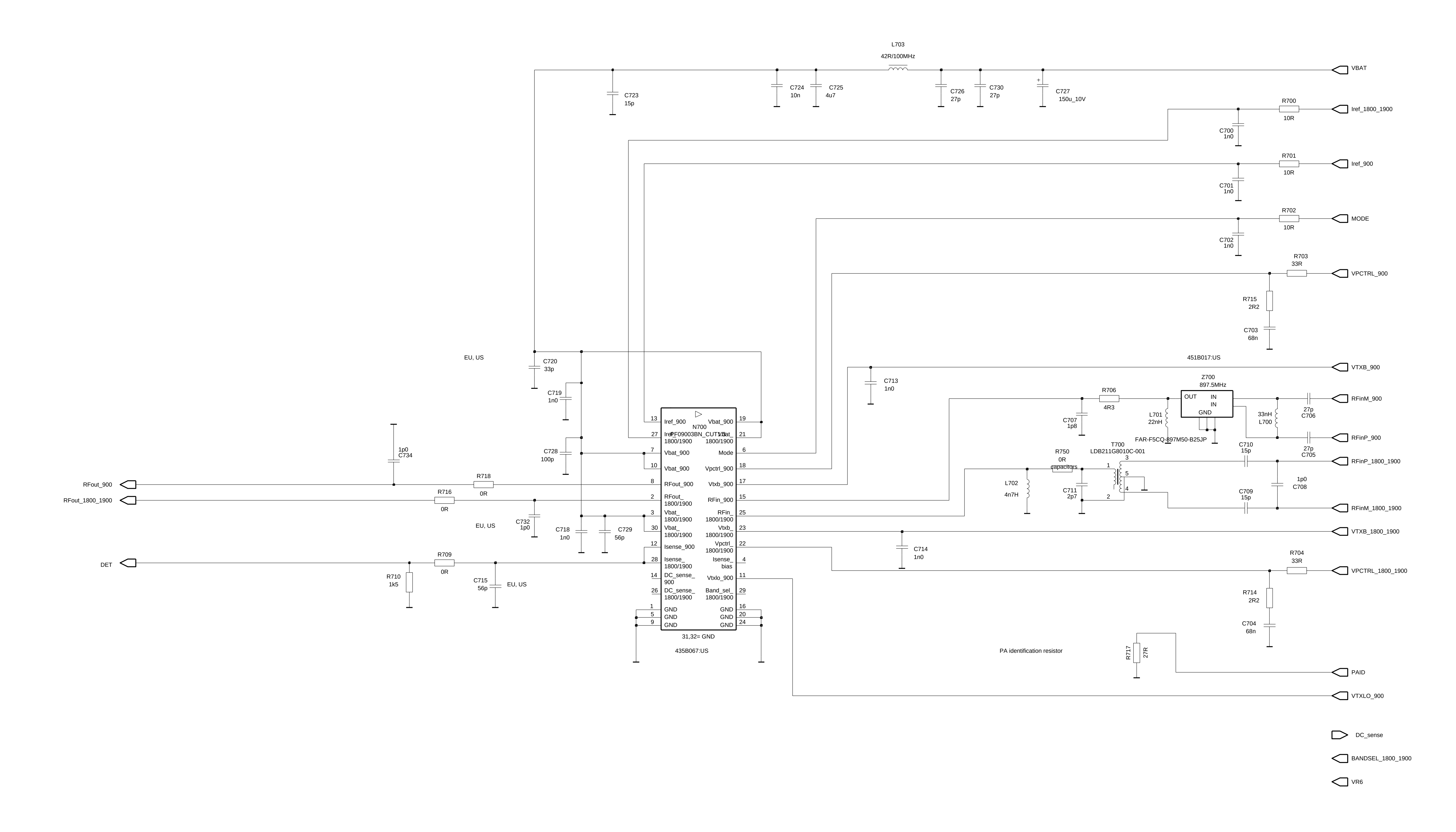
RF shields and vias



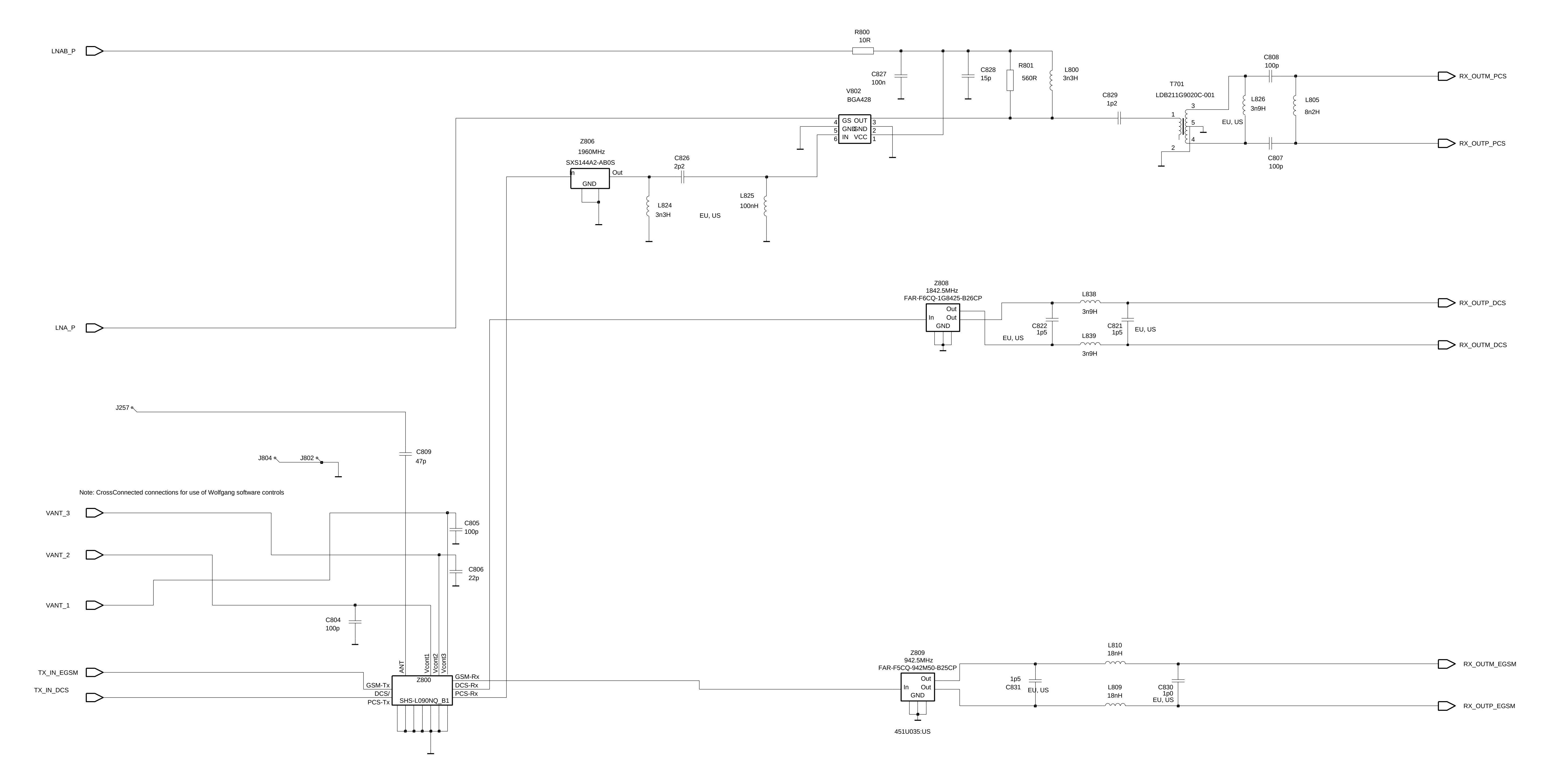
HELGO


N500
HELGO73A
T500
LDB213G6010C-001
G500
ENFVJ5W2S08
G501
NKG3138D
26MHz
C545
4x470p
4x100.0R
600R/100MHz
L=1.8 mm, distance from
adjacent strip = 0.8mm
EU, US
Last references:
C576
R543
L510
T501

Power amplifier and power detection



RX front end and antenna switch



Last references:

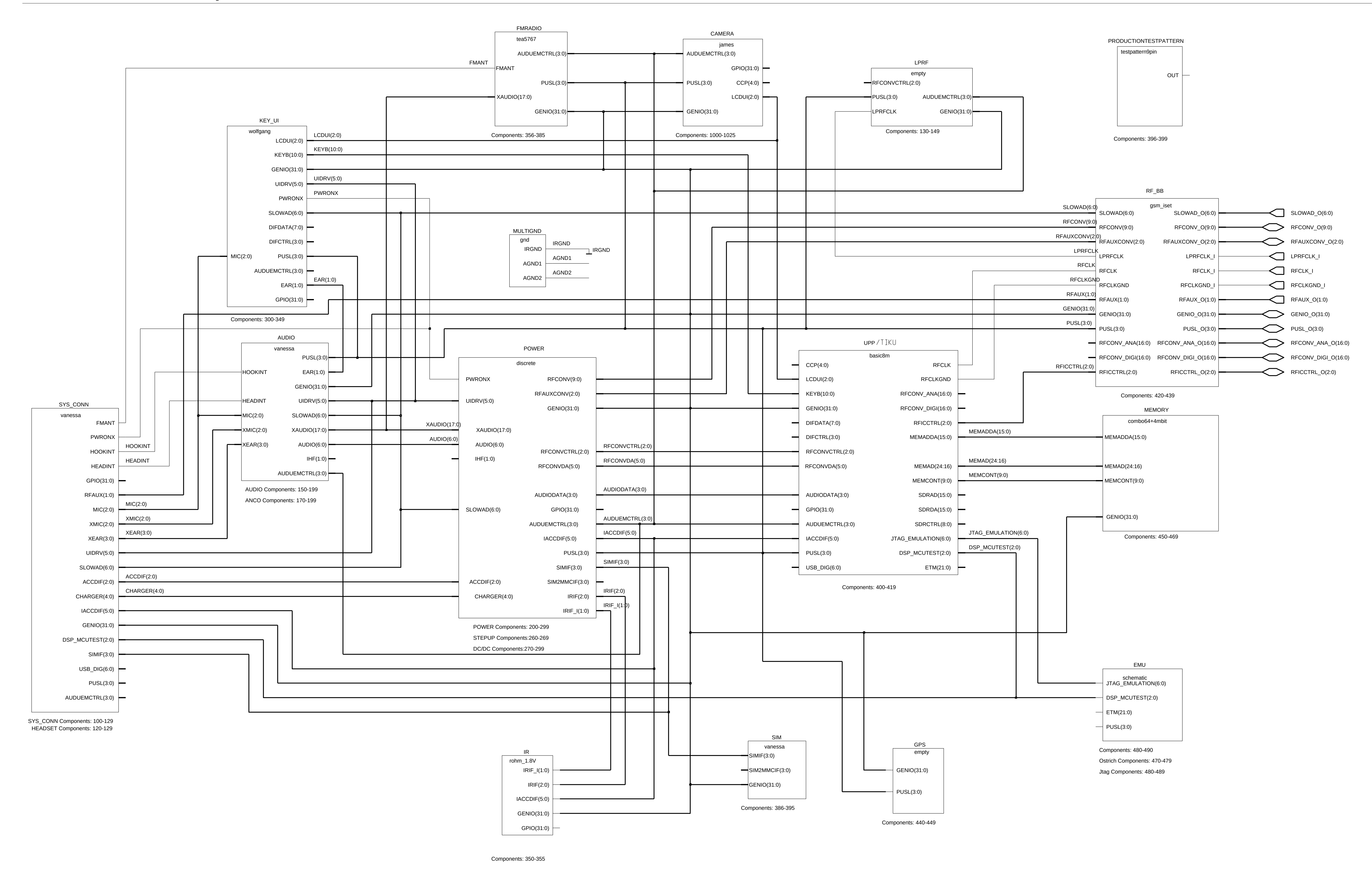
C835

R807

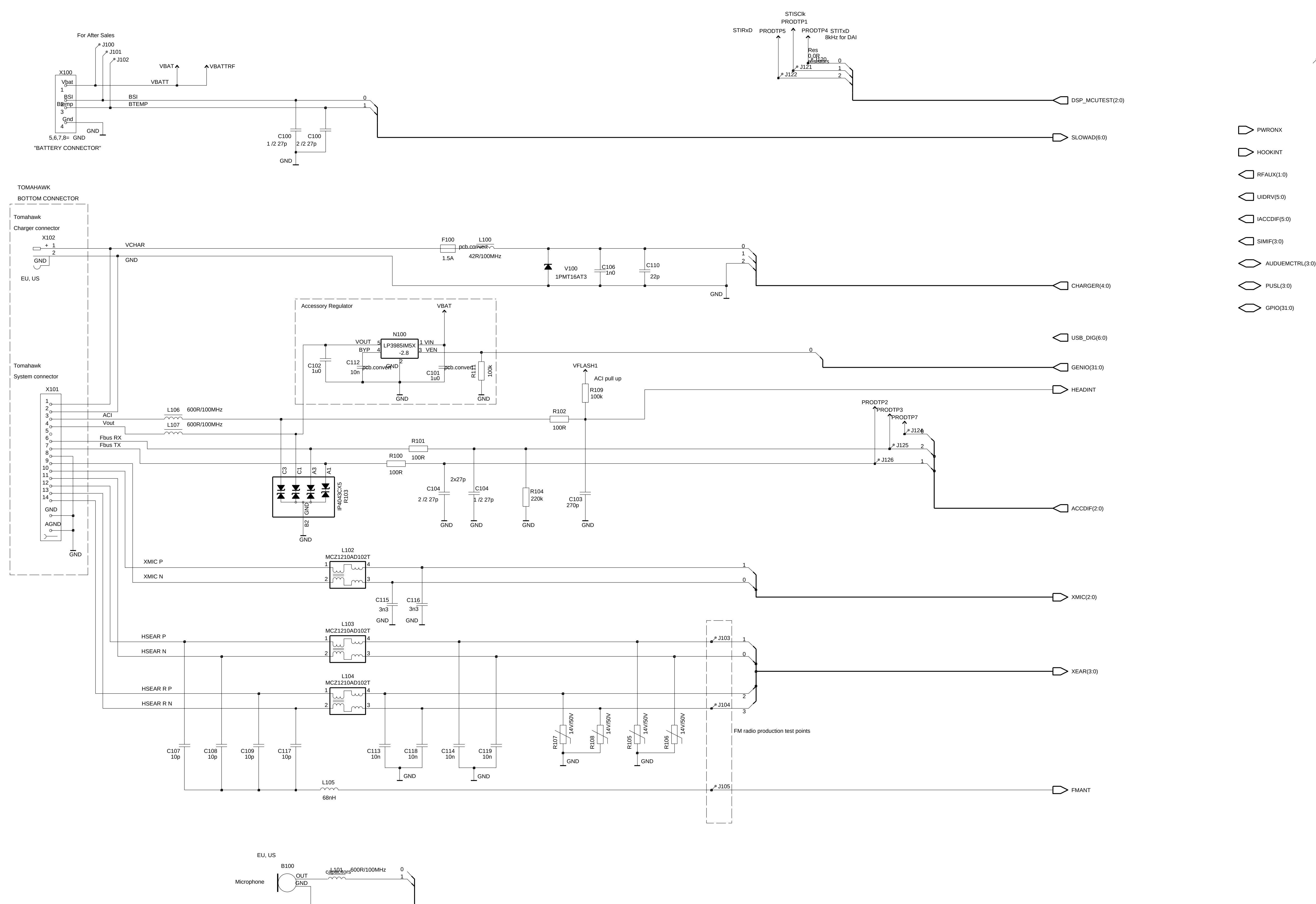
L825

Z806

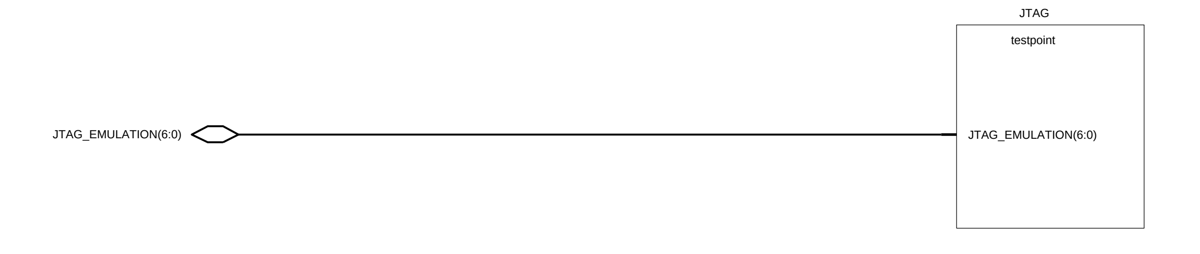
DCT4 Common Baseband (Top)



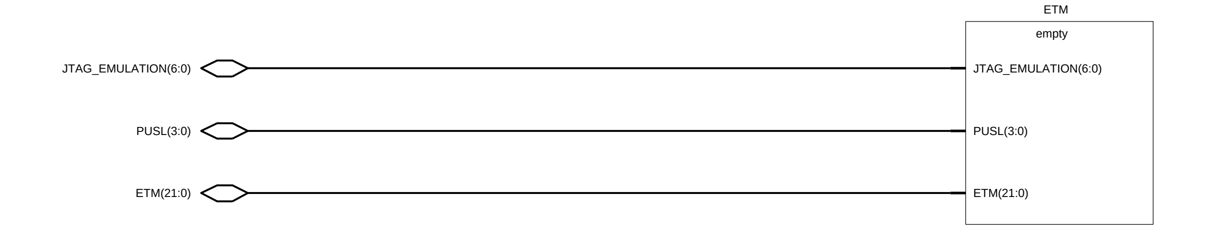
System connector



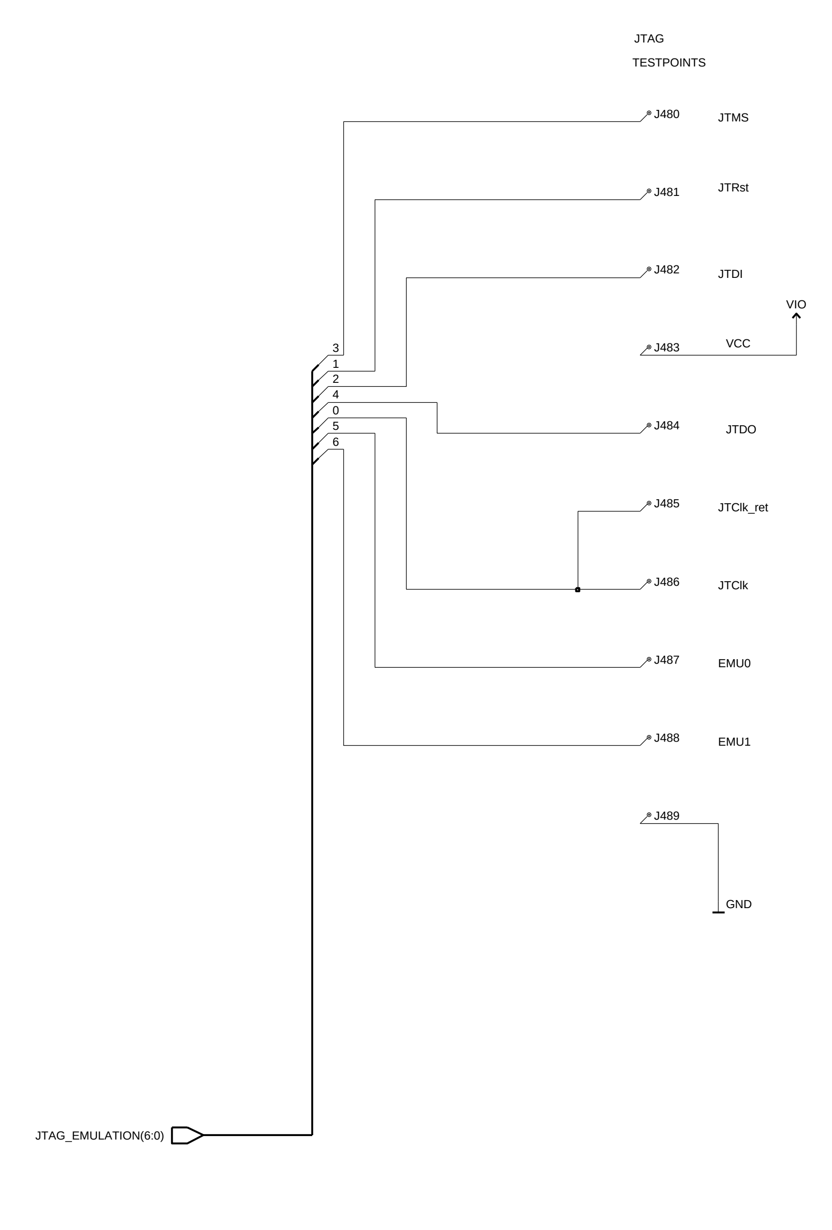
Test and emulator interface



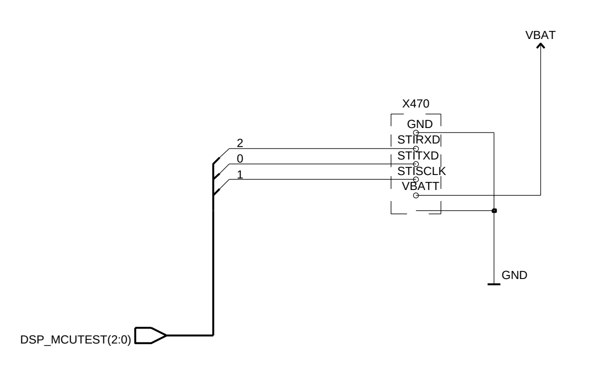




Testpoints for JTAG emulator



Connector based Ostrich test interface



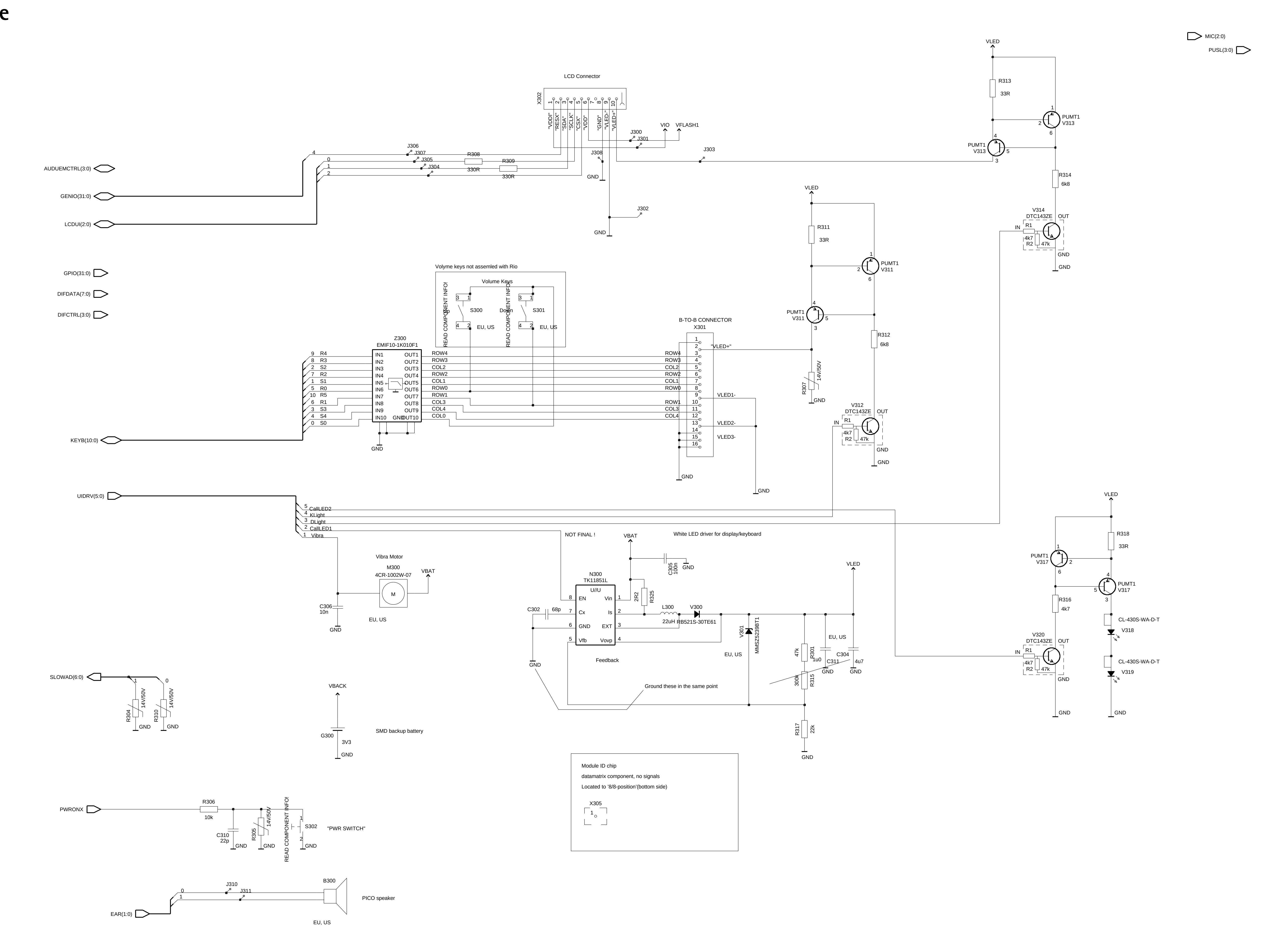
Empty ETM

PUSL(3:0)

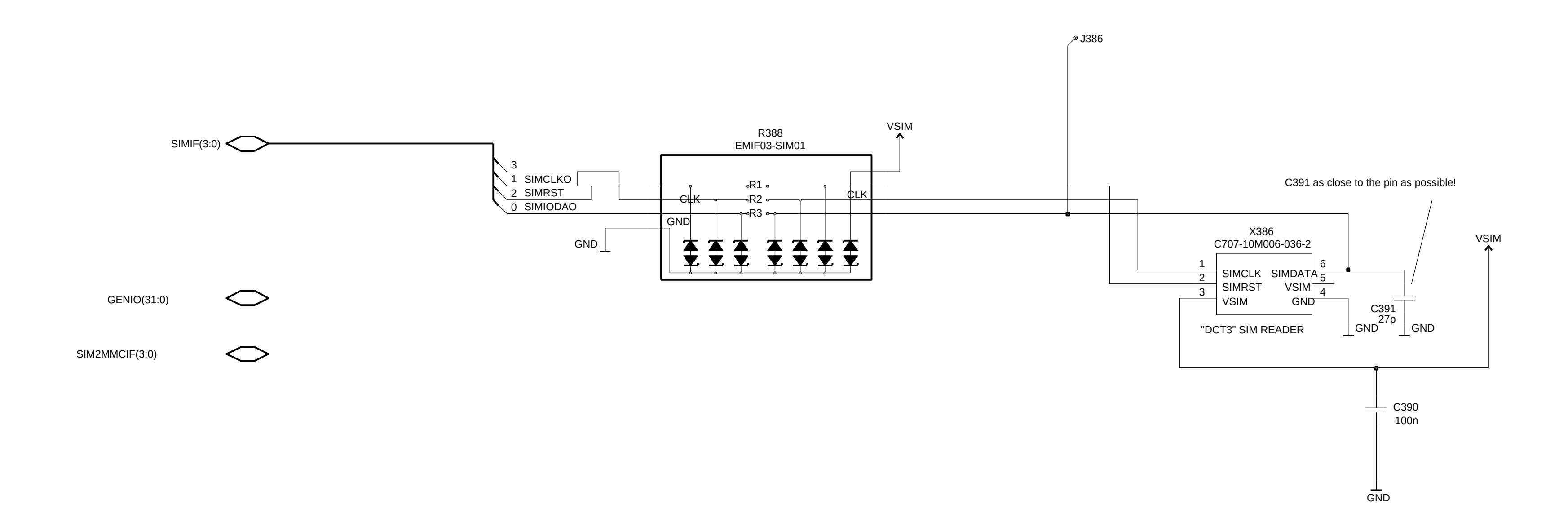
JTAG_EMULATION(6:0)

ETM(21:0)

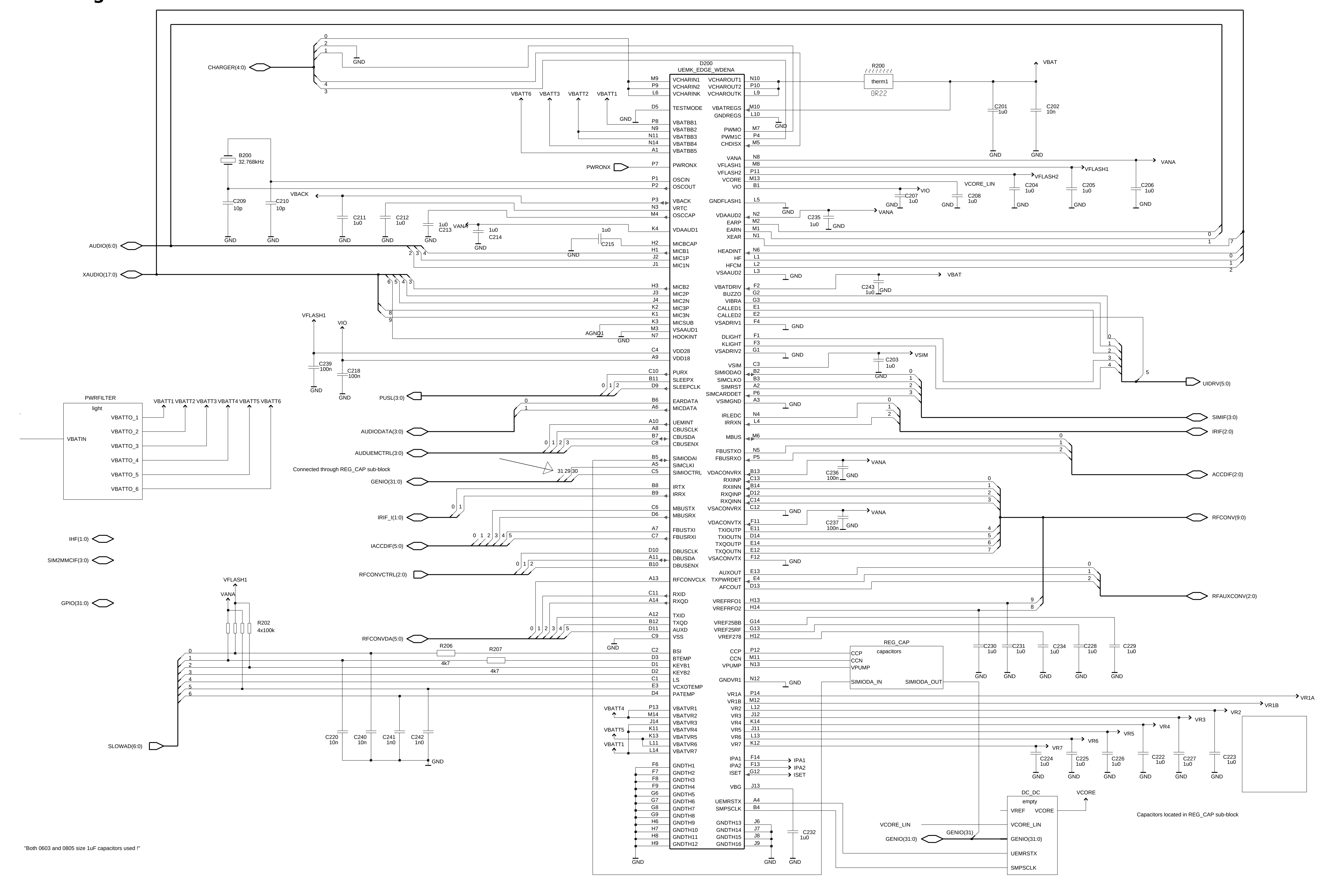
User Interface



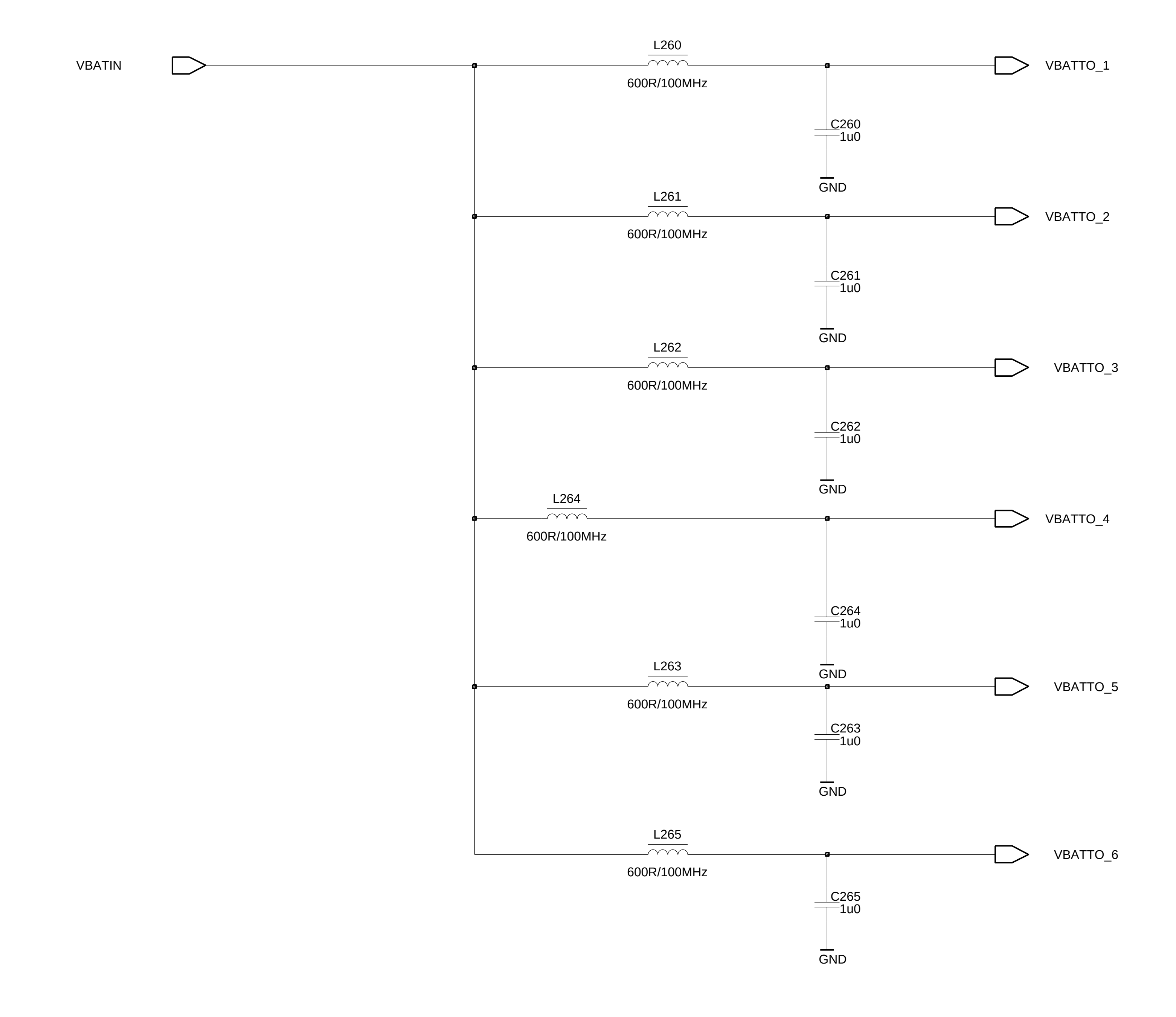
SIM reader


J386
SIMIF(3:0)
3
1 SIMCLKO
2 SIMRST
0 SIMIODAO
R388
EMIF03-SIM01
VSIM
CLK
R1
R2
R3
CLK
GND
GND
C391 as close to the pin as possible!
X386
C707-10M006-036-2
VSIM
SIMCLK
SIMRST
VSIM
SIMDATA
VSIM
GND
"DCT3" SIM READER
C391
27p
GND
GND
GENIO(31:0)
SIM2MMCIF(3:0)
C390
100n
GND

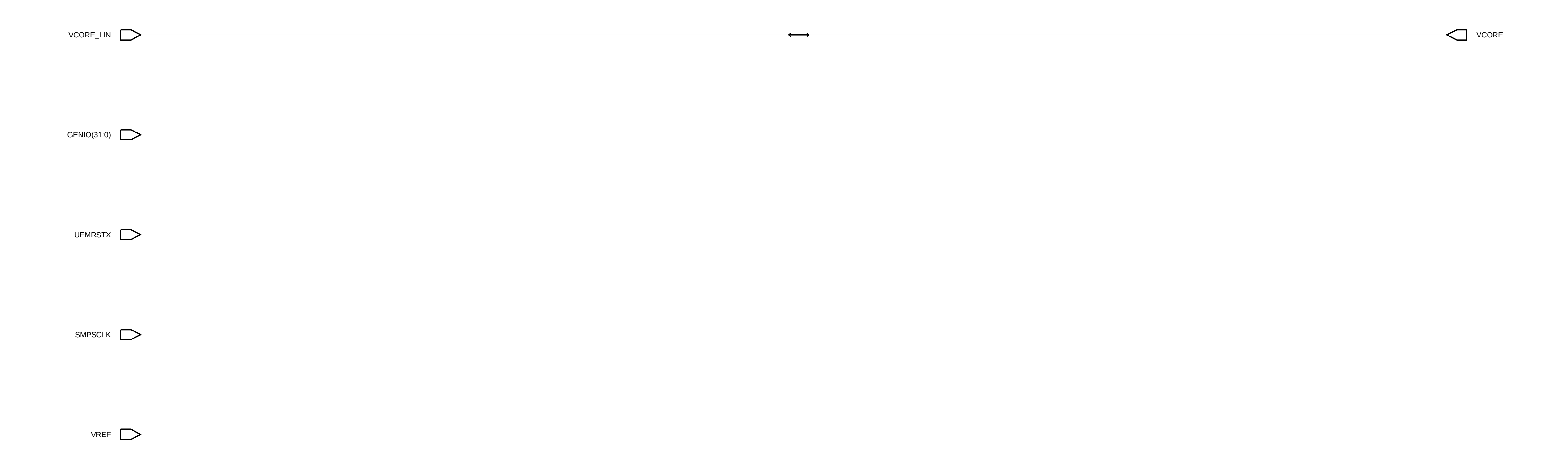
Discrete power management



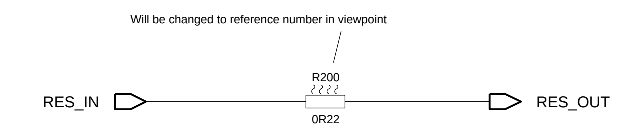
Light filtering



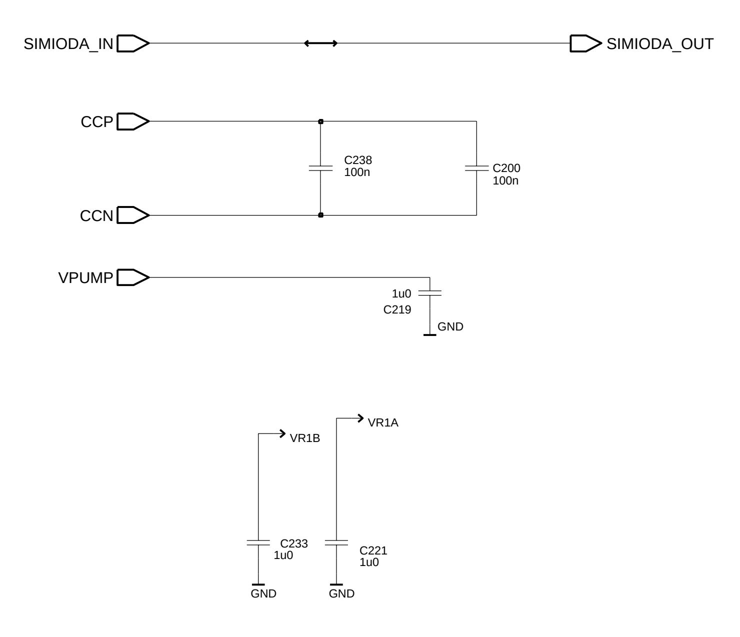
DC/DC converter



PWR resistor

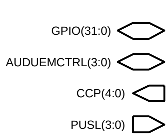


For old discrete power users



Camera

NOTE! New reference numbers 970-999, usage must be checked from RF!



LCDUI(2:0)
GENIO(31:0)
LCDCamTxDa
LCDCamClk
1
0
J970 J971 J972 J973
3
27
28
26

D970
STV0900A_V3.2
A10 CE
D8 CLK
A6 RSTN
J1 MSCL
K4 MSDA
E8 SSCL
F10 SSDA
C6 DAS
G8 TXDA
G10 RXDA
H8 CSX
H10 DACLK
F1 RDP
G1 RDN
F3 RQP
G3 RQN
K5 RB
D1 TQP
E1 TQN
D3 TDP
E3 TDN
C1 TB
A9 PLLVDD
A8 PLLVSS
K7 VDD2.8V
TM1 C8
TM2 B10
TM3 C7
TPio0 C5
TPio1 C10
TPio2 J10
TPio3 A3
TPio4 B1
TPio5 A5
TPio6 H1
TPio7 K2
TPio8 K1
TPio9 A1
TPio10 A2
GND
DC2 K8
DC3 F8
DC1 H6
VDD1.8V C3
VDD1.8V D10
VDD1.8V H3
VDD1.8V H7
VDD1.8V K6
VDD1.8V K10
A4,A7,C4,H4,H5,E10,K3,K9= GND

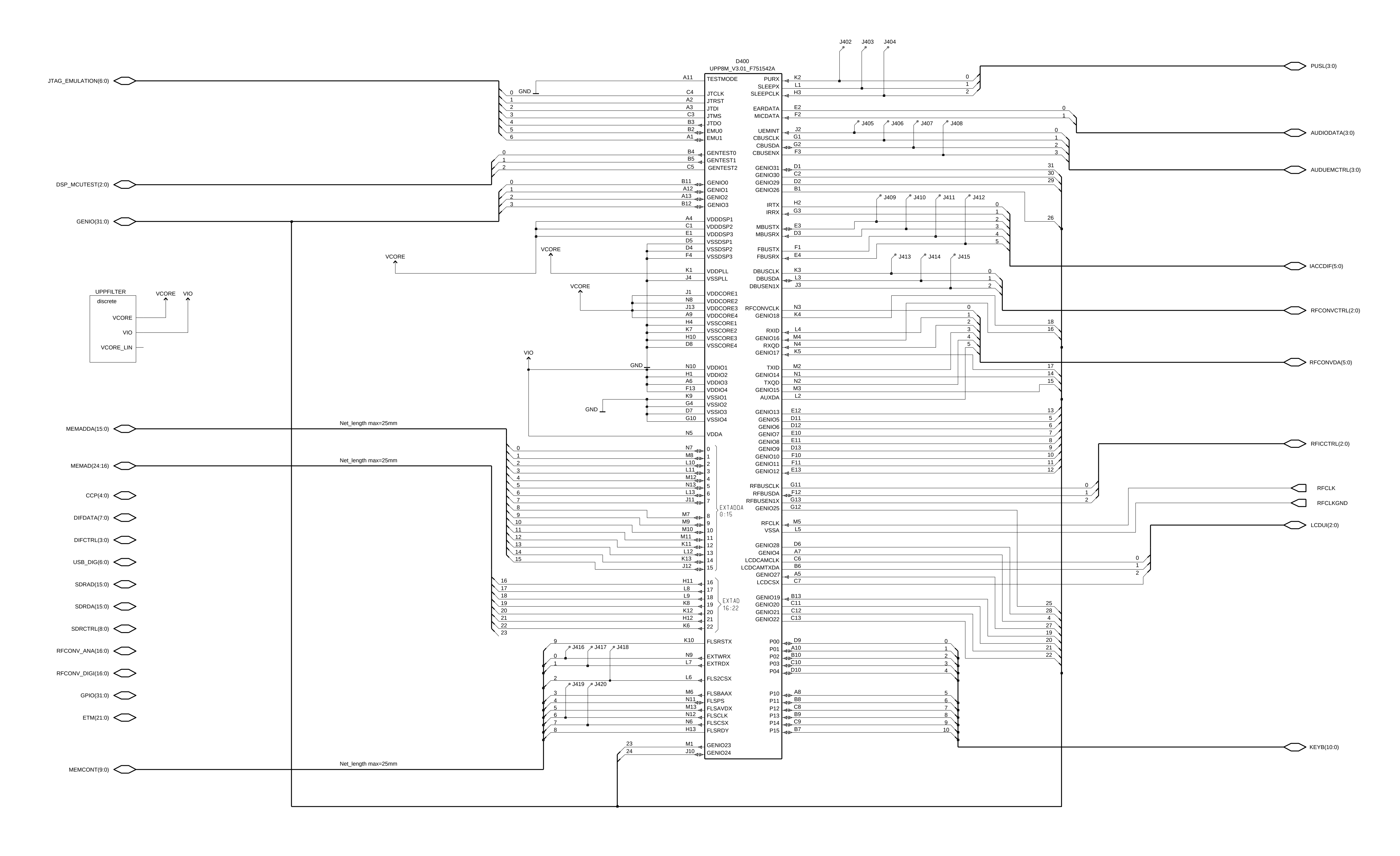
R973 15k GND
VCAMDIG C980 10n GND
VFLASH2 C981 10n GND
R974 100R
R975 100R
R972 10k
C972 10n GND
C977 10n GND
C975 10n GND
C976 10n GND
C979 10n GND
C978 100n GND
VCAMDIG

VCAMDIG VCAMDIG
R970 4k7
R971 4k7
VFLASH2
C971 27p GND
C970 100n GND

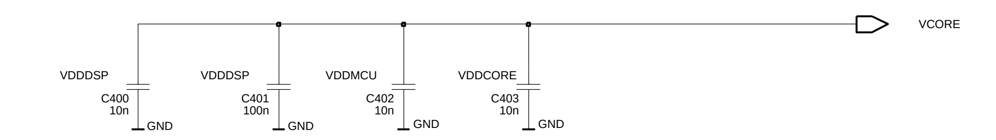
X970
CLE9014-01E
1 SHIELD DGND 14
2 AGND CCPDATAP 13
3 VANA CCPDATAN 12
4 XSHUTDOWN VDIG 11
5 EXTCLK CCPCLKP 10
6 CCISCL CCPCLKN 9
7 CCISDA DGND 8
SHIELD PADS
GND GND
XSHUTDOWN
EXTCLK
CCISCL
CCISDA
VCAMDIG
C973 1u0 GND
C974 27p GND
CCPCLKN
CCPCLKP
CCPDATAN
CCPDATAP

1.8V Regulator
Not Assembled
VBAT VIO
R980 0R EU, US
VCAMDIG
N970 IN
ON_OFF OUT
BYPASS
LP2985ITLX -1.8
GND
C982 1u0 GND
GND
C983 2u2 GND
C984 2u2 GND

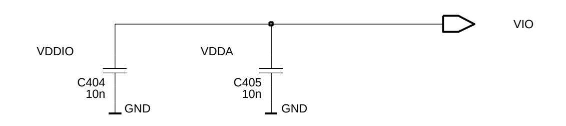
UPP 8M implementation



Discrete decoupling capacitors for UPP



VCORE_LIN



No LPRF interface in this product

GENIO(31:0)

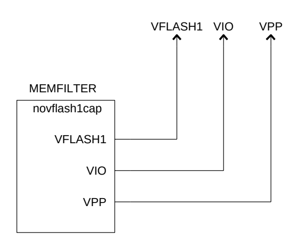
AUDUEMCTRL(3:0)

PUSL(3:0)

RFCONVCTRL(2:0)

LPRFCLK

Combo memory 64+4Mbit



MEMEXTENSION
empty
MEMADDA(15:0)
MEMAD(24:16)
MEMCONT(9:0)
GENIO(31:0)
FLS2CSX

MEMWING
empty
GENIO(31:0)
MEMAD(24:16)
MEMADDA(15:0)
MEMCONT(9:0)
FLS2CSX
FLSCSX

GENIO(31:0)
23

D450
K5U64418TM-TG90
FLASHM 4Mx16
SRAM 256kx16

MEMAD(16) B2
MEMAD(17) A9
MEMAD(18) B8
MEMAD(19) A8
MEMAD(20) B3
16 A 20
FLASH/SRAM
MEMAD(21) A2 A21/_LB
B7 _WP/_CS
FLASH
MEMCONT(6) A4 CLK RDY A1
MEMCONT(9) B6 _RESET
B9 _CEF
SRAM
MEMAD(22) A10 UB
COMMON
MEMCONT(5) B4 _AVD
MEMCONT(0) A6 _WE
MEMCONT(1) C10 _OE
MEMCONT(4) B5 PS
NC 1 E451
NC 2 E452
NC 3 E453
NC 4 E454
NC 5 E455
NC 6 E456
NC 7 E457
NC 8 E458

MEMAD(24:16)

D10
ADDRESS/DATA I/O
0
1 D9
2 C7
3 C6
4 D5
5 D4
6 C3
7 C2
8 C9
9 C8
10 D7
11 D6
12 C5
13 C4
14 D2
15 D1

VPP
PRODTP6
MEMCONT(3)
R450
4k7
E450

MEMCONT(9:0)
MEMCONT(8)

A5,B1,D8= VIO
A7=VPP
A3,B10,C1,D3= GND

MEMADDA(15:0)

Memory extension

GENIO(31:0)

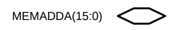
FLS2CSX

MEMAD(24:16)

MEMCONT(9:0)

MEMADDA(15:0)

Empty wing sheet



MEMAD(24:16)

GENIO(31:0)

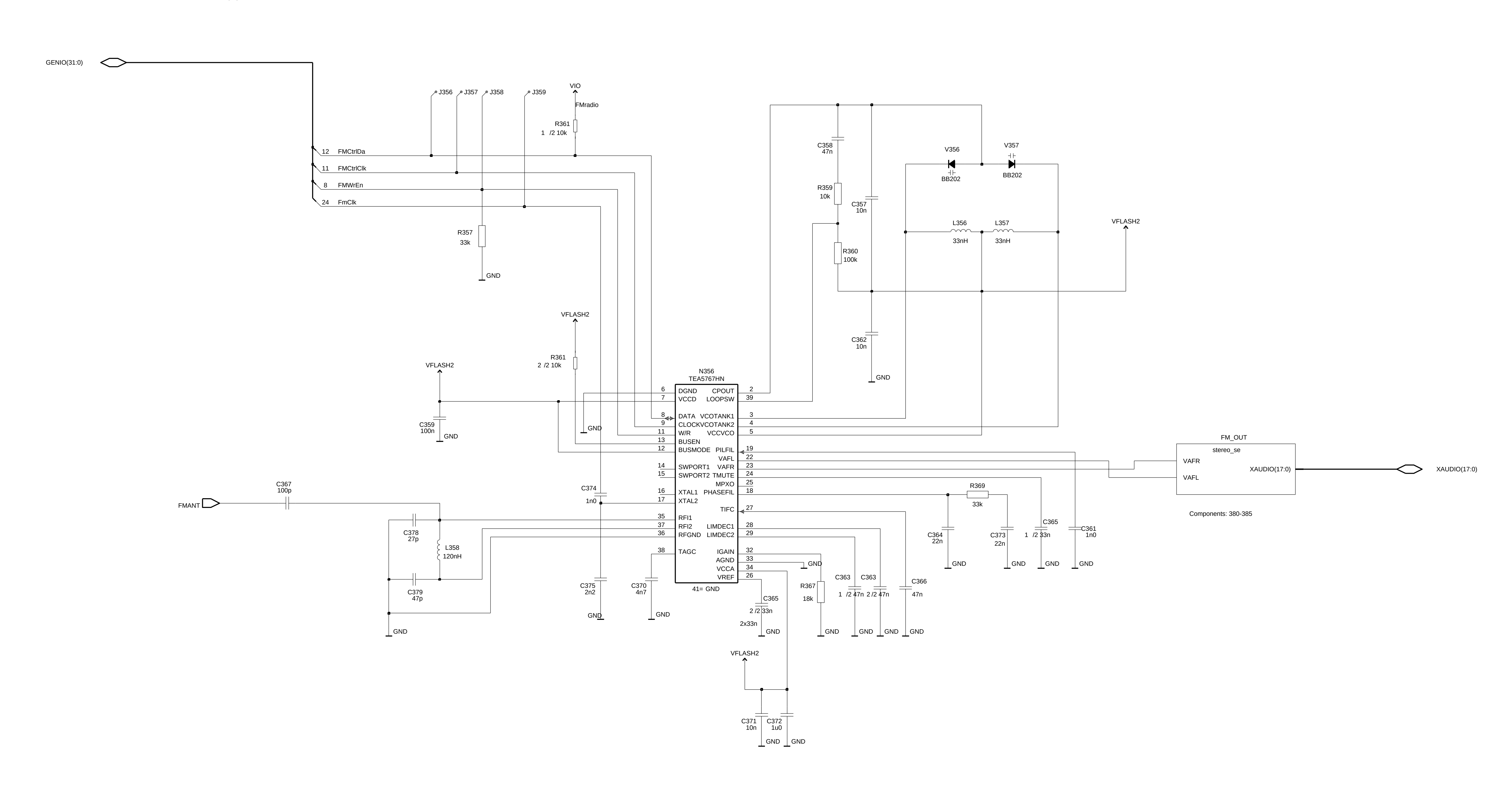


Discrete capacitors for memory without VFlash1





FM radio unit

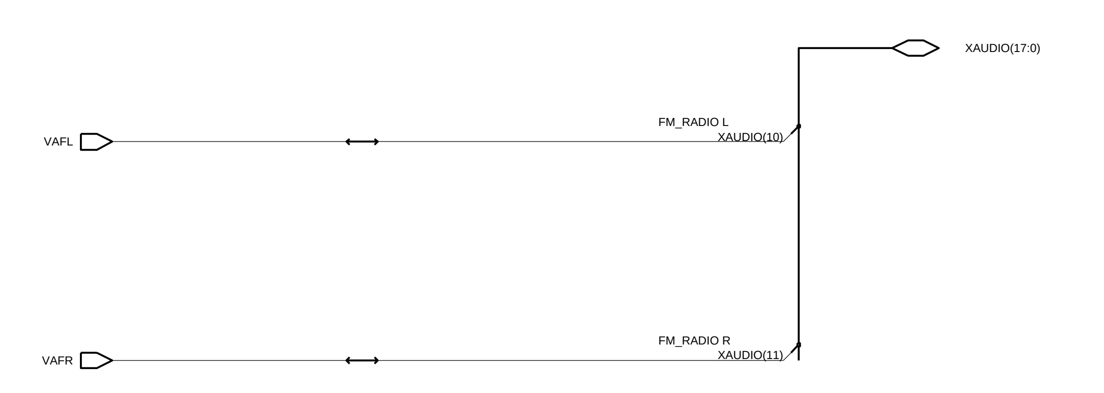


Notice:

C374 (1n0) and C375 (2n2) are configured for 32kHz reference clock

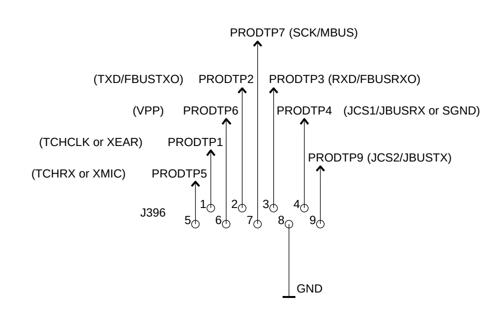
If reference clock is 6.5MHz, use C374 (3p9) and C375 (10p)

FM radio unit

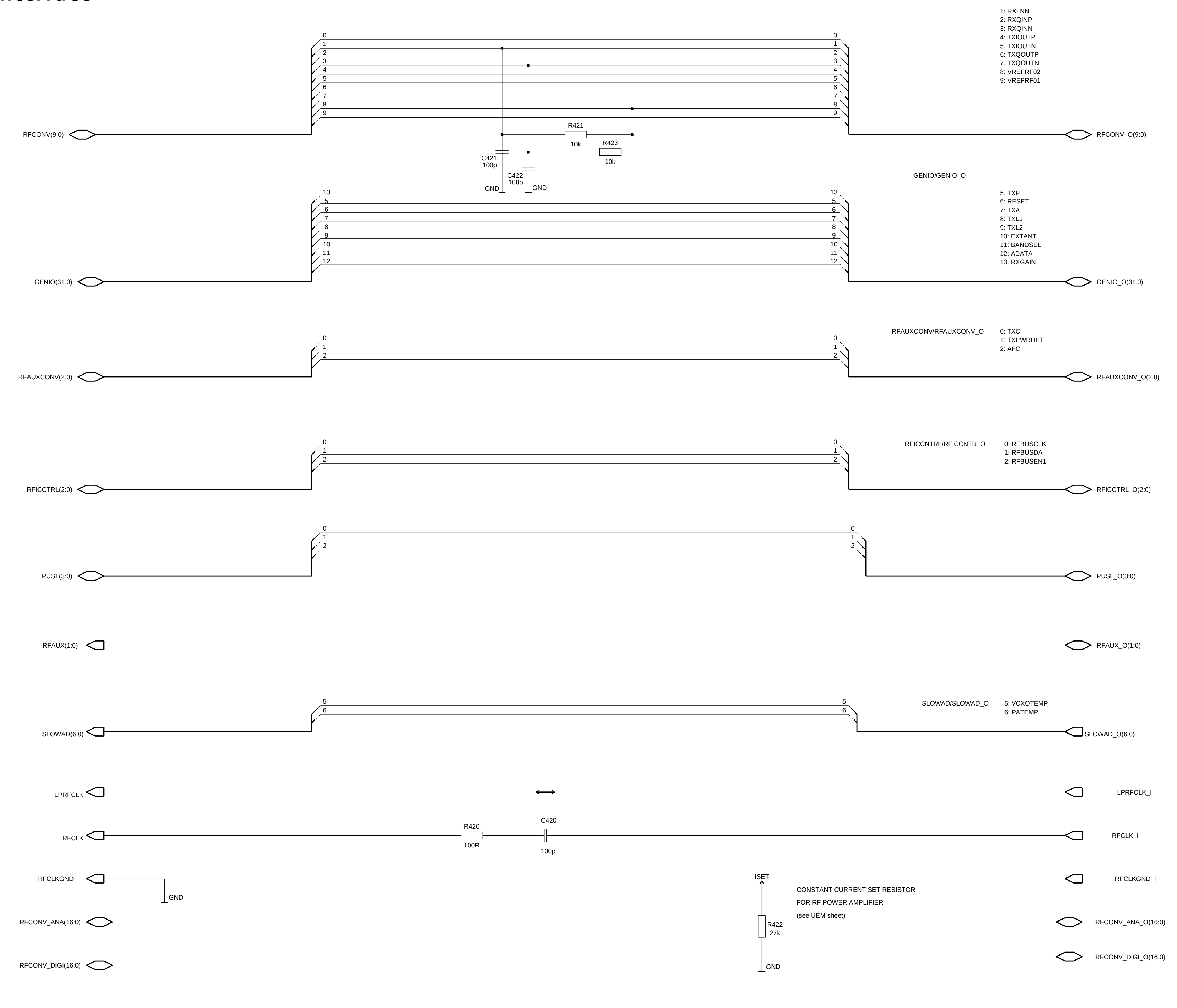


9 pin production test pattern

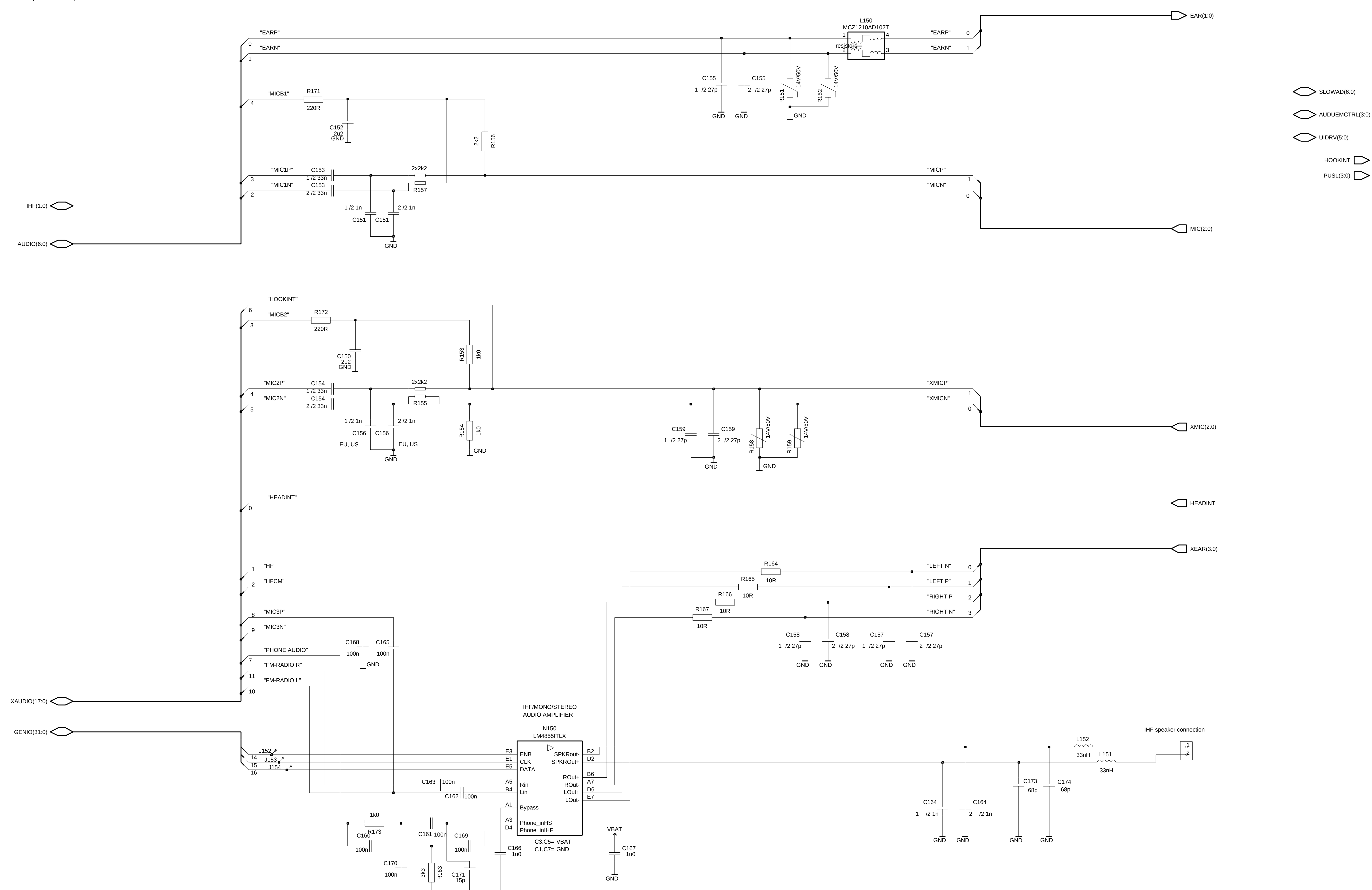
OUT



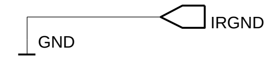
GSM RF-BB interface



Audio



MultiGND symbol bypass



AGND1
GND

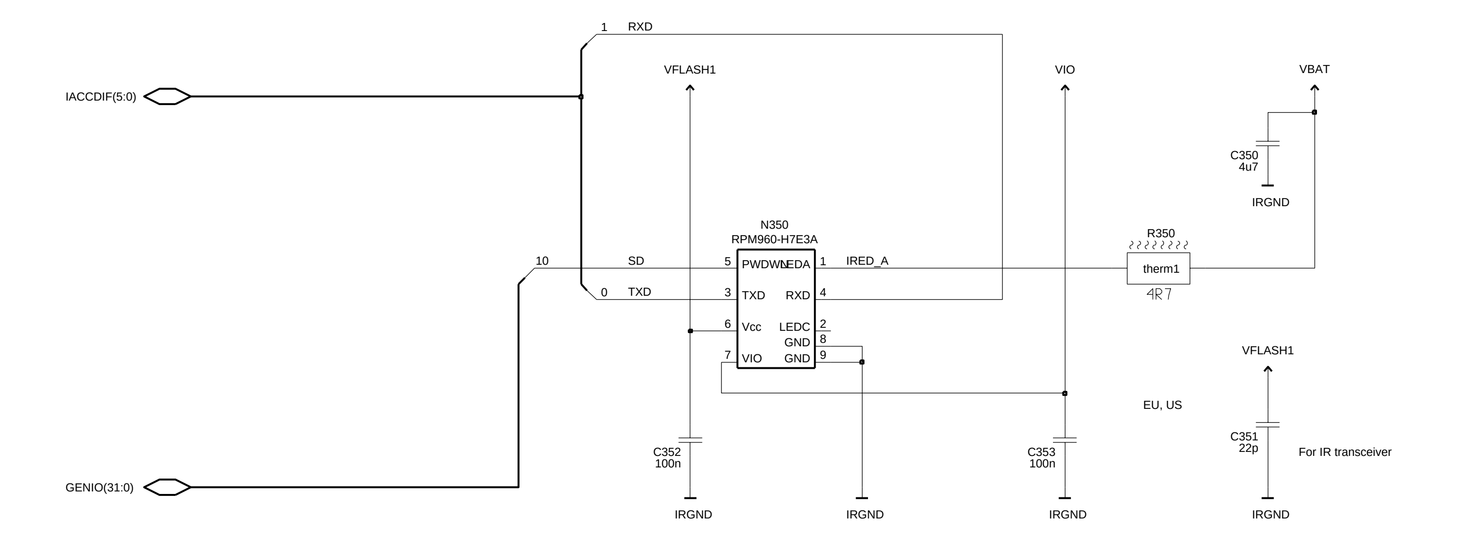
AGND2
GND

GPS empty sheet

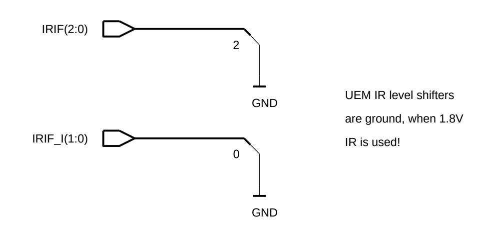


GENIO(31:0)

Rohm IR module 1.8V



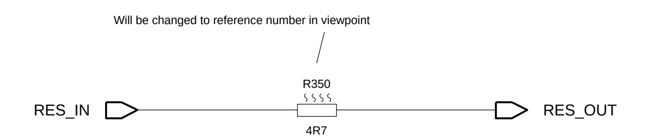
GPIO(31:0)



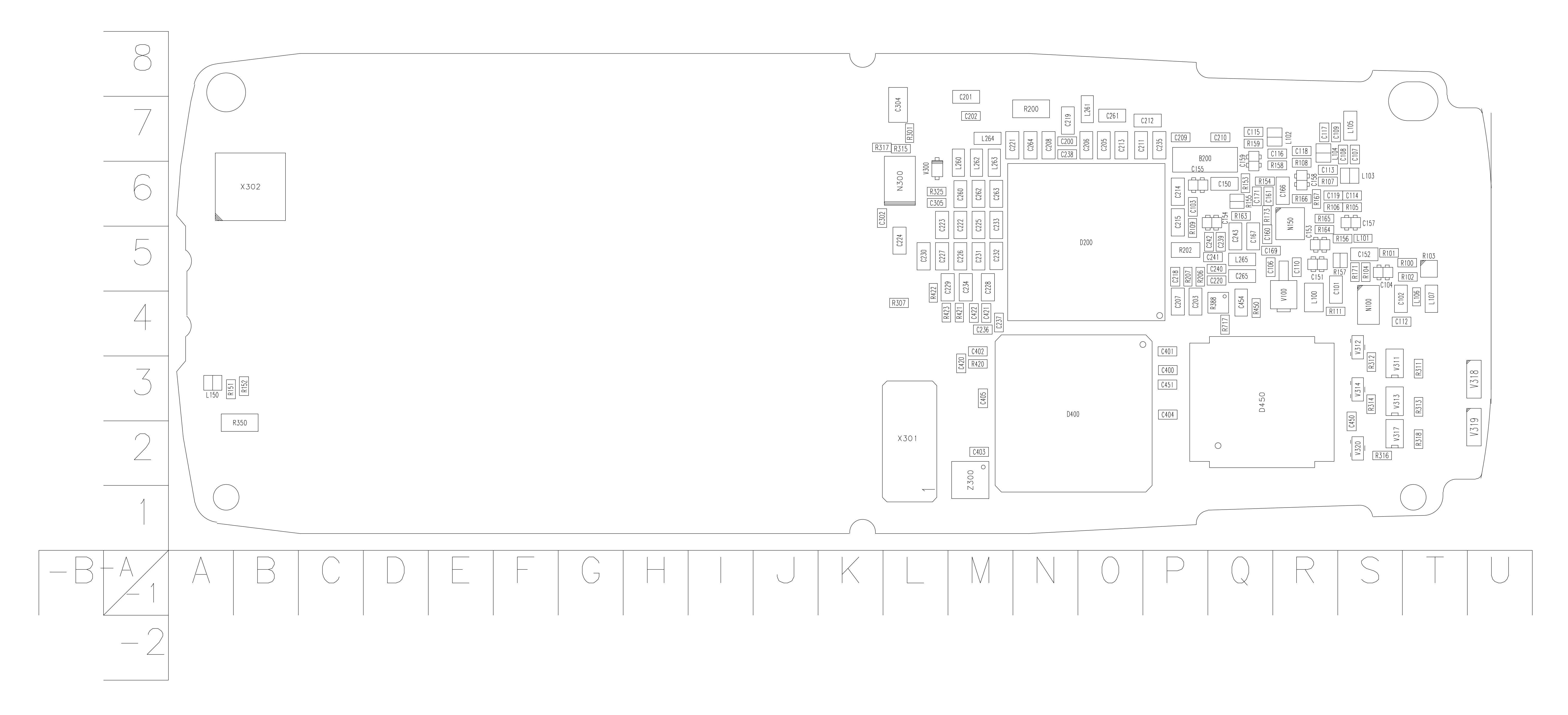
Used referenses

C 350 - 353
N 350
R 350

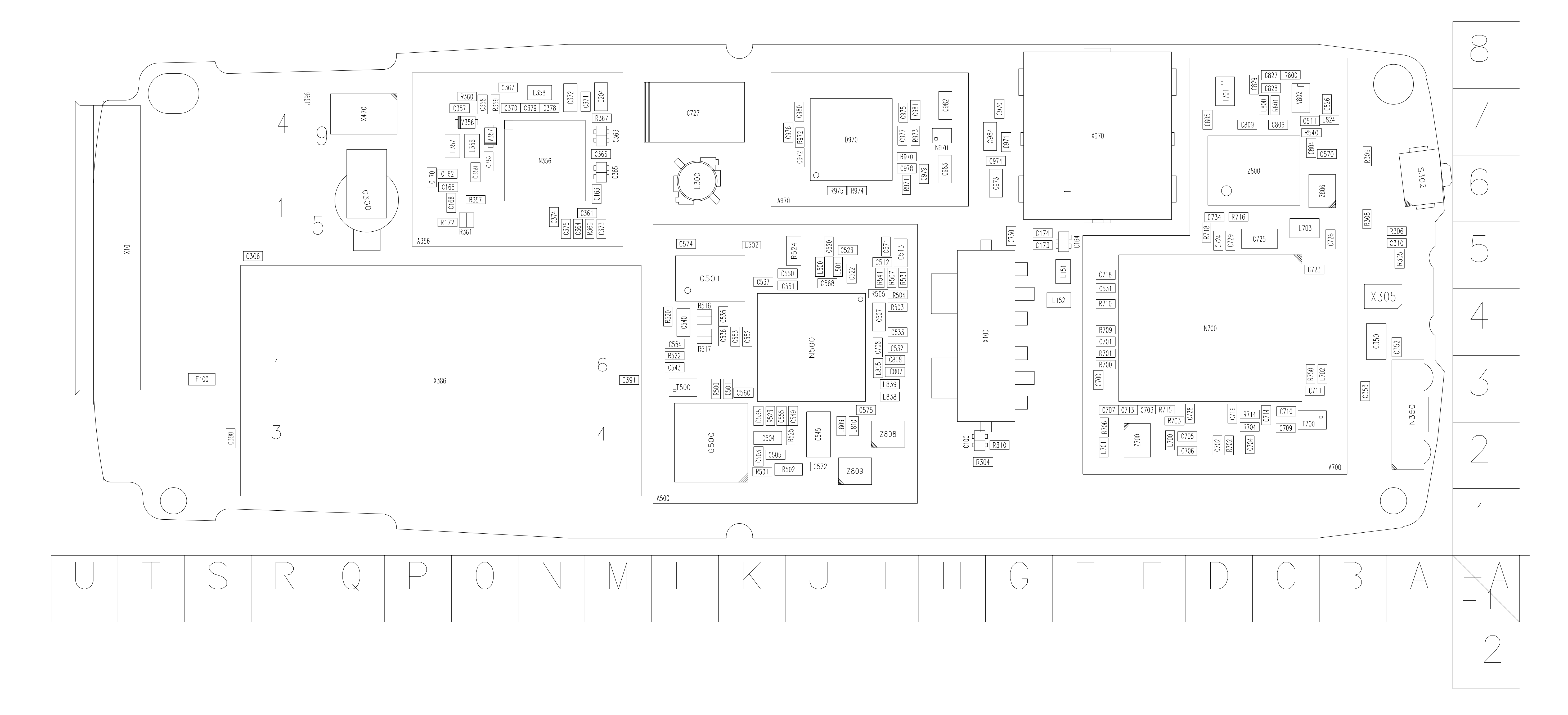
IR resistor


Will be changed to reference number in viewpoint
R350
RES_IN
RES_OUT
4R7

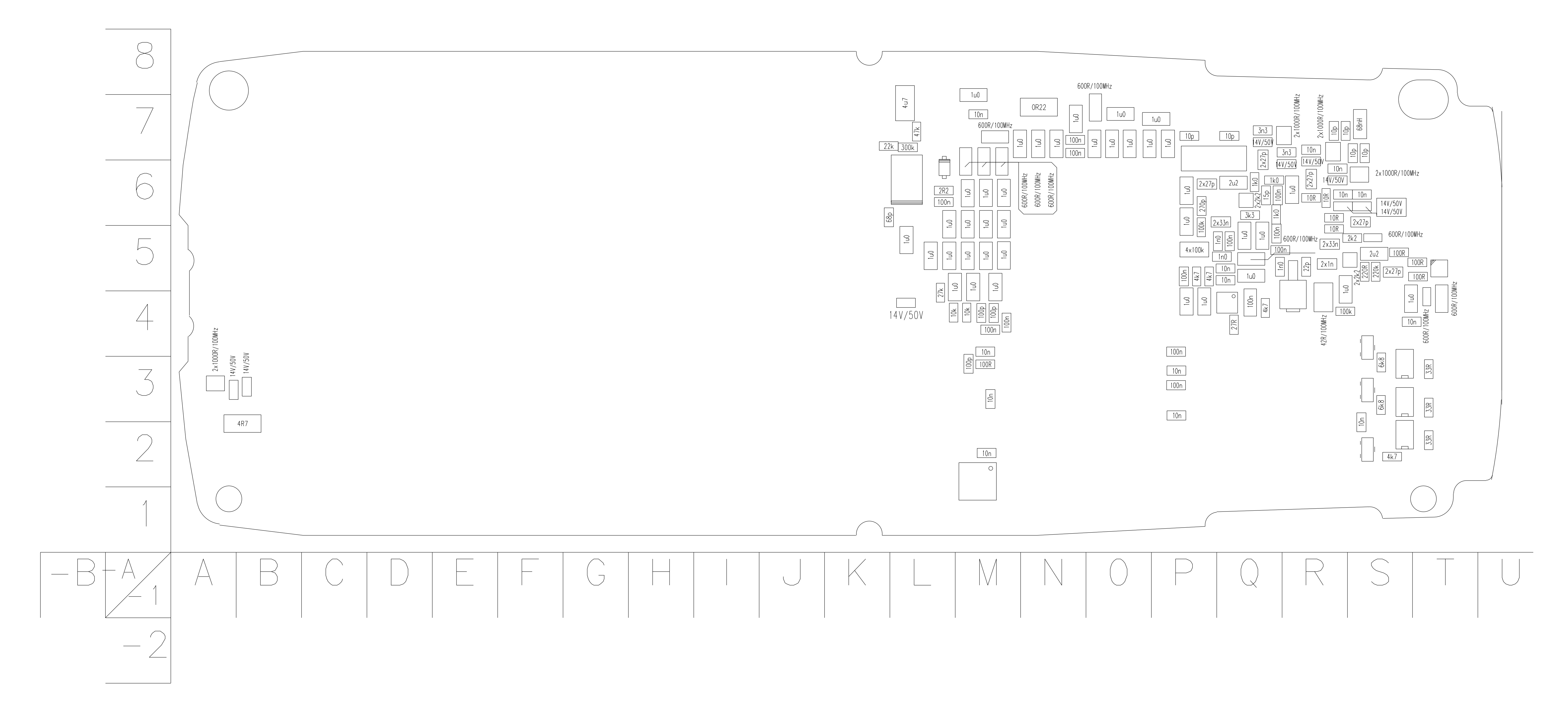
Layout


8
7
6
5
4
3
2
1
-1
-2
-B
-A
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
T
U
X302
X301
D200
D400
D450
N300
N100
N150
B200
Z300
V318
V319
R350
L150
R151
R152
R200

Layout



Layout



Layout

